# **A Review On I2C Serial Communication**

Prachi Ikhar<sup>1</sup>, Prof. S. N. Rawat<sup>2</sup>

Department of Electronics and Telecommunication <sup>1, 2</sup> Bhivarabai Sawant Institute of Technology and Research, Pune, India

Abstract- Inter-Integrated Circuit, abbreviated as I2C is a serial bus short distance protocol developed by Philips Semiconductor. Serial communication is mainly used by embedded system to communicate with different peripheral and now a day's embedded system is growing very rapidly. Serial communication plays very important role in embedded system. Serial communication protocol have characteristic of high speed and low data cost. The number of serial communication protocol a are used like Universal Receiver Transmitter (UART), Control Access Network (CAN), Universal Serial Bus (USB), Serial Peripheral Interface (SPI) and Inter IC Protocol (I2C). Less number of wires for interconnection is used by I2C for implementing on FPGA it provided the flexibility to use it according to the application. This paper provides reviews use of I2C protocol with prelude of FPGA implementation.

Today a system is connected to a number of devices and makes the communication smooth and fast, I2C protocol is considered as one of the very best. [5]

#### I. INTRODUCTION

An embedded system physical size get reduce by reducing the size of transistor. But the number of interconnected devices also increases which increases the problems. Philips Electronics design the protocol to overcome all these problems in the communication between different Integrated IC called Inter IC protocol.I2C protocol is used by different devices such as keyboard, memory, cell phone ,TV, etc. Physically I2C bus consists of two wires SCL and SDA. These are active high, bidirectional and half duplex in nature. I2C is multi master bus it means that more than One IC is capable for data transpiring .All the devices connected to SCL and SDA line having unique address. Any devices act as transmitter or receiver depending on the nature of the device. Here master initiate the data transper and data get exchange between master and slave. SCL line controls all the communication between master and slave. By using clock stretching SCL and SDA line avoid collision.SCL and SDA line are bidirectional lines.

Figure1 shows that both the lines connected to positive supply voltage via a pull up resistor. By default both lines are high. . The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. They are pulled-up to the logic 'high' level by resistors connected to a single positive supply, usually +3.3 V or +5 V. All the connected devices have open collector driver stages that can transmit data by pulling the bus low and high impedance. [6]



Fig 1. Schematic Representation of Devices with I2C Bus

#### **II. LITERATURE SURVEY**

Sahu et al. developed inter IC protocol for data surveillance purpose. Data surveillance is very important application to monitor people or sensors.I2C is used for data surveillance because it could make system efficient, accurate, flexibility, and low development cost. They designed a protocol in VHDL and interface with OV7620 single chip CMOS VGA color digital camera.[1]

Shah et. Al designed inter IC protocol using system verilog and FPGA. Design mainly includes master design and slave design. Master design was implemented in medium size FPGA and its computation was performed on 32 bit Microblaze processor which performs all encryption and decryption. Design contained different register as pre scale register, command register, status register, transmit and receive register.[2] Researcher developed an interface model for scale free network using inter-IC bus protocol which includes master and slave design. Master was made up of different blocks as initiator, address block, write block, read block, clock generator. Initiator tested whether data bus was free to use or not. Address bit was transmitted by address block bit by bit to SDA line and after completion of address it reset SDA line to high position. Transmission and reception functions were performed by write and read block. All functions of master are governed by clock generator block. Slave was made up of design of monitor, address block,

receiver and transmitter. Monitor function was same as initiator in master which sense the SCL and SDA line whether it is in use or not.

## **III. SYSTEM DEVELOPMENTS**

Master and slave have to be design to develop the I2C and that design is develop using the Active HDL 9.3 software.



Fig 2. Propose diagram of I2C

Master and slave are the two units in design and these are embedded into FPGA. Only two lines are there to communicate with each other. The FPGA can work as dedicated interface between the different devices for the communication.

## **IV. CONCLUSION**

This paper is review on implementation of I2C protocol. I2C is one of the types of serial communication protocol which reduces the number of wire for communication, minimum pin count and easy controlling. Implementing I2C on FPGA is useful for minimal coding, fast operation and for data processing.

#### REFERENCES

- A.Sahu, R. Mishra, P.Gour, "An Implementation of I2C using VHDL for Data Surveillance", International Journal on Computer Science and Engineering May 2011, pp – 1857 – 1865
- [2] S. Sobhan, S. Das and I. Rahman, "Implementation of I2C Using System Verilog And FPGA", International Conference on advancement in electronics and power Engineering Bangkok December 2011.
- [3] A. Khan, A. Thakare, "FPGA Based Design & Implementation of Serial Data Transmission

Controller" International Journal of Engineering Science and Technology 2010, pp 5526 – 5533.

- [4] P.Venkateswaran, M. Mukherjee, A. Sanyal, R. Nandi ,"Design And Implementation Of FPGA Based Interface Model for Scale Free Network Using I2C Bus Protocol On Quartus II 6.0", International conference on computer and devices for communication and Devices for Communication 2009.
- [5] J.Lazaro, A.Astarloa, A. Zuloaga, "I2C: A xxxsecure serial chip to chip communication protocol" journal of system architecture 57 pp.206-213 2011
- [6] The I2C Bus specification version 2.1 January 2000 Philips.