# Input Vector Monitoring Concurrent BIST Architecture using Modified SRAM Cells

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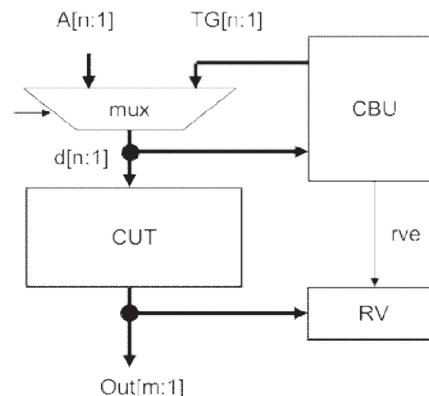
***Abstract-*** *Input vector monitoring concurrent BIST performs two modes of operation, normal mode and test mode During test mode the test generator value is compared with higher order bits and the output is given to comparator circuit. During normal mode the inputs to the CUT are driven from the normal inputs. The modified SRAM is used to reduce the switching activity hence the dynamic power dissipation can be reduced. The output is verified by response verifier (RV) and the fault is identified using testing. The operating speed is faster since the operation is carried out as parallel process and it is suitable for all the type of IC's.*

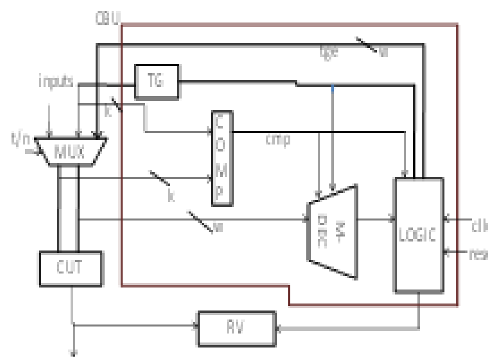
***Keywords-*** Comparator, Test generator enable, Concurrent BIST unit, Modified SRAM, logic module, concurrent test, response verifier.

## I. INTRODUCTION

Built-in-self test (BIST) techniques constitute a class of schemes that provide the capability of performing testing with high fault coverage. Hence, they constitute an attractive solution to the problem of testing VLSI devices. BIST techniques are typically classified into offline and online. Offline architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV).The bits are classified into higher and lower order bits. During the normal mode the vector that drives the inputs of the CUT is driven from the normal input vector. It operates in two modes. When T/N=0 it operates in normal mode, if T/N=1 the operation is said to be in test mode. The modified decoder and the modified SRAM are used. The decoder operation is carried along with TGE and CMP values based on which the decoding operation occurs. Modified SRAM is used not only for storing purpose but also for reducing the switching activity. This leads to reduction in dynamic power dissipation. The output from both the logic circuit and the CUT are captured and it is verified using response verifier (RV). The process is carried out parallel hence speed of operation is more.




## II. BLOCK DIAGRAM DESCRIPTION




### A. HARDWARE TEST PATTERN GENERATOR:

This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs. As the test pattern generator is a circuit (not equipment) its area is limited. So storing and then generating test patterns obtained by ATPG algorithms on the CUT using the hardware test pattern generator is not feasible. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2n-1, if there are n flip-flops in the register) as possible.

### B. DECODER:

A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used

to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. Decoding is necessary in applications such as data multiplexing, 7 segment display.

### C. COMPARATOR:

comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes . The circuit, for comparing two n-Bit numbers, has inputs. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and the wiring complexity. The wiring complexity is determined by the number of connections and their lengths.All these charactersistics may vary from one logic style to another and thus proper choice of logic style is important.

### D. SRAM:

SRAM is a type of semiconductor memory that uses bitable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data eminence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used with applications such as moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption in the region of a few micro-watts.

## III. IMPLEMENTATION AND RESULTS

### POWER ANALYSIS:

| Supply voltage | Logic block | Circuit under test |
|---|---|---|
| Average power | 2.162147x10^-2 | 1.2532x10^-2 |
| Maximum power(static) | 1.741*10^-2 @5.00x10^-6 | 6.367934X10^-3 @5.408X10^-6 |
| Minimum power(dynamic) | 2.862x10^-8@3.781x10^-5 | 11.280X10^-7 |
| PDP | 87n ws | 1.1280nws |
| EDP | 0.43 pws | 50.7465 pws |

Table 1:Power analysis

### FORMULA USED:

PDP= power x time ws
EDP= power x (time)^2 ws
Staticcurrent=P=VxI=>I=P/V(or)(v=1.8799x2.5x2.5um^2)
Dynamiccurrent=P=VxI=>I=P/V

### DECODER OUTPUT:

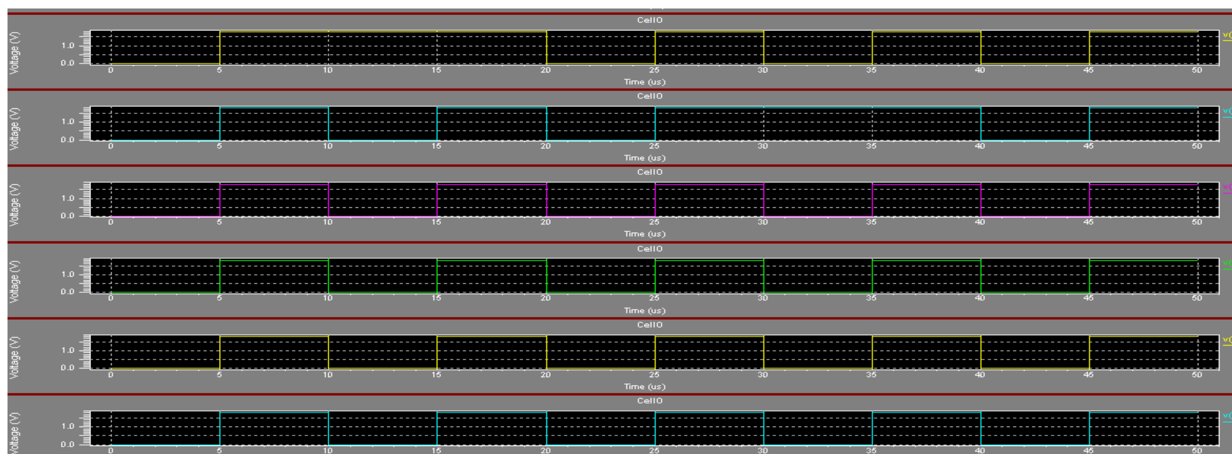


Fig 1: decoder output

**COMPARATOR OUTPUT:**

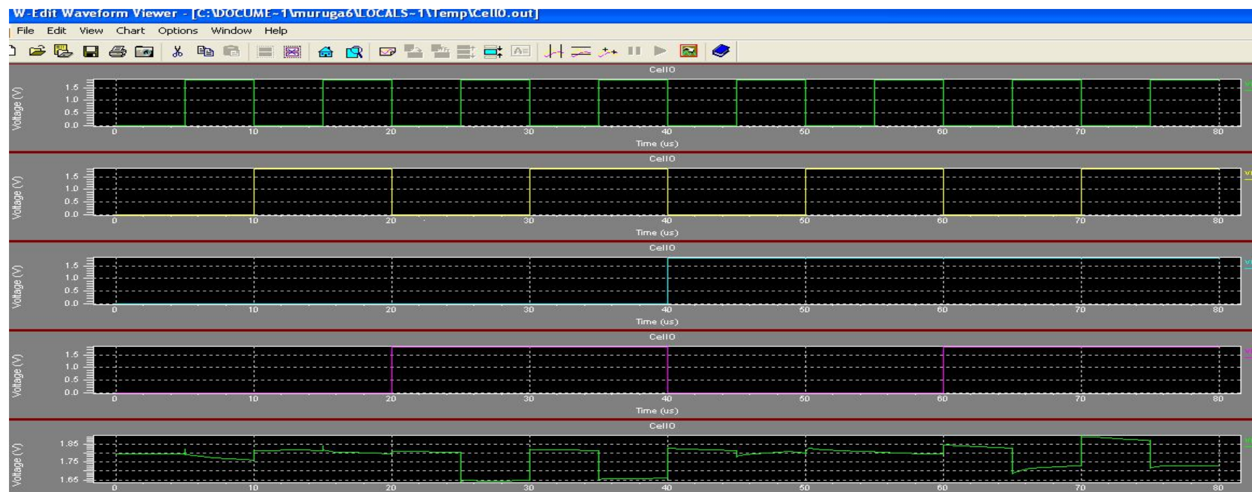



Fig 2: comparator output

**BCUT OUTPUT:**

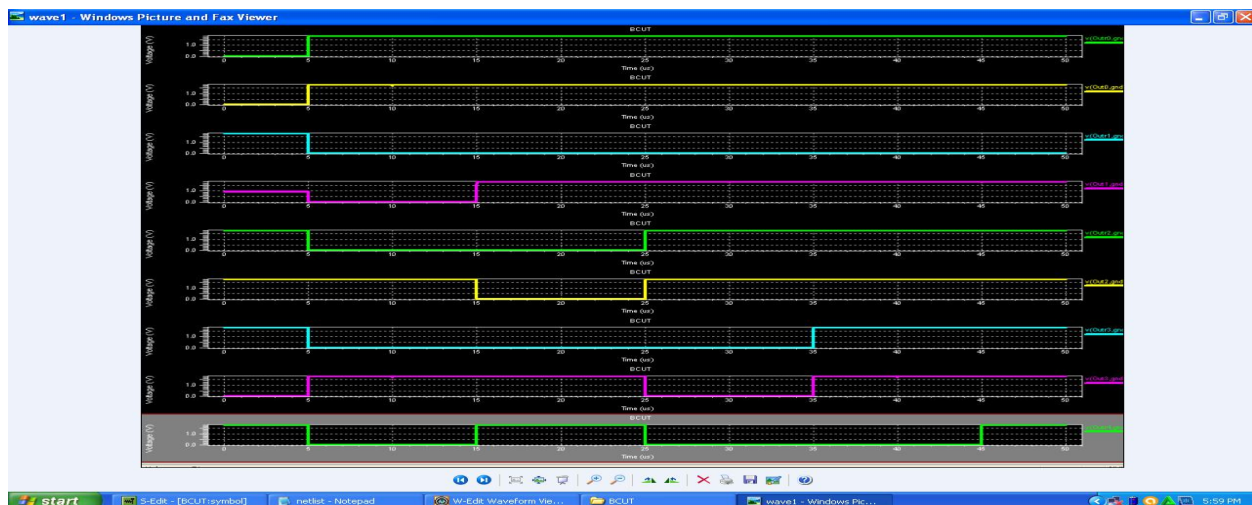



Fig 3:Bcut output

## IV. CONCLUSION

BIST schemes constitute an attractive solution to the problem of testing VLSI devices. Input vector monitoring concurrent BIST schemes perform testing during the circuit normal operation without imposing a need to set the circuit offline to perform the test, therefore they can circumvent problems appearing in offline BIST techniques.The operation is carried out both in normal mode and test mode .During normal mode the outputs from the CUT and logic block are verified using response verifier RV.During test mode tge values are generated and the output is verified based on that values.Based on clock and selection lines the output is executed.

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